

# USEEN1 - Computer Systems Modeling and Verification

## Présentation

### Prérequis

Computer Science or Computer/Electrical Engineering Bachelor.

### Objectifs pédagogiques

Students who take this course will gain an understanding of the concepts and theories of computer-aided formal specification and verification, and learn how to use and write formal verification tools.

## Programme

### Contenu

Most of the course is devoted to high-level semantic design and code-level properties. The emphasis is put on executable specifications and verification tools based on the following methods:

- Static analysis and type checking
- Design-by-contract and property-based testing

Static and dynamic verification in particular are compared in this course, with a focus on tools and prototype development:

- **Preliminaries**
  - Imperative programming and unit testing
  - Functional programming and logic
- **Part I: static analysis**
  - Specification: typing rules (deductive system)
  - Implementation: mode-based extraction of functional code
- **Part II: dynamic verification**
  - Specification: design-by-contract
  - Implementation: self-testing and property-based testing

### Modalités de validation

- Contrôle continu
- Examen final

### Description des modalités de validation

Attendance and participation in lessons (50%) and written final exam (50%).

Mis à jour le 12-02-2024



**Code : USEEN1**

Unité spécifique de type mixte  
6 crédits

**Responsabilité nationale :**  
EPN05 - Informatique / 1